



(19) Europäisches Patentamt  
European Patent Office  
Office européen des brevets



(11) Publication number:

**0 430 274 A2**

(12)

## EUROPEAN PATENT APPLICATION

(21) Application number: 90122947.6

(51) Int. Cl.5: H01L 21/331, H01L 21/225

(22) Date of filing: 30.11.90

(30) Priority: 01.12.89 JP 313724/89  
01.12.89 JP 313725/89

(43) Date of publication of application:  
05.06.91 Bulletin 91/23

(84) Designated Contracting States:  
DE FR GB Bulletin 1A/F

(71) Applicant: SEIKO INSTRUMENTS INC.  
31-1, Kameido 6-chome Koto-ku  
Tokyo 136(JP)

(72) Inventor: Aoki, Kenji, c/o Seiko Instruments Inc.  
31-1, Kameido 6-chome Koto-ku, Tokyo(JP)  
Inventor: Akamine, Tadao, c/o Seiko Instruments Inc.  
31-1, Kameido 6-chome Koto-ku, Tokyo(JP)  
Inventor: Kojima, Yoshikazu, c/o Seiko Instruments Inc.  
31-1, Kameido 6-chome Koto-ku, Tokyo(JP)

(74) Representative: Fleuchaus, Leo, Dipl.-Ing. et al  
Melchiorstrasse 42  
W-8000 München 71(DE)

(54) Method of producing bipolar transistor.

(57) The method of producing a bipolar transistor comprised of collector, base and emitter regions disposed sequentially on a semiconductor substrate. A semiconductor layer is deposited on the collector region. The semiconductor layer is cleaned to expose an active surface. An impurity source gas is applied to the exposed active surface while heating the substrate to form an impurity adsorption layer. The impurity is diffused into the semiconductor layer to form the base region. Another semiconductor layer is deposited on the base region. This semiconductor layer is cleaned to expose an active surface. Another impurity source gas is applied to the exposed active surface while heating the substrate to form another impurity adsorption layer. This impurity is diffused into the semiconductor layer to form the emitter region.

**EP 0 430 274 A2**

rity is effected from a diffusion source in the form of the impurity adsorption layer into the semiconductor film layer to form the base region. The impurity concentration and diffusion depth of the base region are controlled quite accurately by suitably setting the amount of the adsorbed impurity and the diffusion condition such as substrate temperature and heating time.

In order to achieve the above noted second object of the invention, according to the second aspect of the invention, the bipolar transistor is produced by sequential steps of depositing a semiconductor film layer on a previously formed base region, cleaning a surface of the semiconductor film layer to expose an active surface, applying a gas containing an impurity component to the active surface while heating the substrate to form an impurity adsorption layer, and diffusing the impurity into the semiconductor film layer to form an emitter region.

Preferably, the adsorption step is carried out by applying a diborane gas containing a boron impurity component to a silicon semiconductor film layer to form a boron adsorption layer. Consequently, there is formed an emitter region diffused by the P type impurity of boron to produce the PNP bipolar transistor.

In the second aspect of the invention, the impurity gas is applied to the semiconductor film layer deposited on the base region while heating the substrate so as to form the impurity adsorption layer on the active surface. Then, the solid-phase diffusion is effected from a diffusion source composed of the impurity adsorption layer into the semiconductor film layer to thereby form an emitter region. This impurity diffusion is confined within the semiconductor film layer which constitutes the emitter region, hence the impurity density distribution is not affected in the base region disposed under the emitter region.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A - 1F are a process step diagram of an NPN bipolar transistor;

Fig. 2 is a block diagram of a production apparatus for use in the bipolar transistor fabrication;

Fig. 3 is a process sequence chart of the bipolar transistor fabrication;

Fig. 4 is an impurity density profile in a base region of the bipolar transistor;

Fig. 5 is a graph showing the relation between a boron peak density and an impurity gas application condition; and

Figs. 6A - 6F are a process step diagram of a PNP bipolar transistor.

#### DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, the description is given in detail for preferred embodiments of the inventive method of producing bipolar transistors in conjunction with the drawings. Figs. 1A - 1F are a process step diagram of an NPN bipolar transistor. In the Fig. 1A step, a collector region 2 is formed on a semiconductor substrate 1 composed of silicon. The collector region 2 has a double layer structure comprised of a first layer 3 of N type and a second layer 4 of N type. The N type first layer 3 contains a high density of N type diffused impurity in order to reduce collector-series resistance of a bipolar transistor. Further, the N type second layer 4 is used to form a PN junction. A field oxide film 5 is formed on the collector region 2 so as to isolate individual bipolar transistors from each other. The field oxide film 5 can be formed, for example, by means of selective thermal oxidation. The field oxide film 5 is provided to surround a device region in which one bipolar transistor is fabricated.

In the Fig. 1B step, the collector region 2 is cleaned over its surface, and thereafter is deposited with a semiconductor film layer 6 composed of silicon. The silicon semiconductor film layer 6 has a significantly small thickness since a base region is to be formed therein in later step. For this, the deposition of the semiconductor film layer 6 can be carried out by, for example, molecular layer epitaxy. By this method, a semiconductor film layer 6 of silicon single crystal can be formed on the collector region 2.

In the Fig. 1C step, the surface of semiconductor film layer 6 is cleaned to expose an active surface. Then, the substrate 1 is applied with a gas such as diborane which contains an impurity component of boron to form an impurity adsorption layer 7 composed of boron element or boron compound. The amount of the adsorbed impurity can be appropriately set by controlling gas pressure of diborane, application time interval and substrate temperature.

In the Fig. 1D step, the adsorbed impurity is diffused into the semiconductor film layer 6. The diffusion is carried out by heating the substrate. The substrate temperature and heating time interval are suitably set so as to substantially uniformly distribute the impurity boron to form a base region 8.

In the Fig. 1E step, an oxide layer 9 is disposed over the substrate surface except each device region. The oxide layer 9 is formed by means of chemical vapor deposition of silicon dioxide and etching thereof. Subsequently, a silicon semiconductor film layer 10 is deposited in a window surrounded by the oxide layer 9. This silicon semiconductor film layer 10 is formed by means of epitaxial growth or chemical vapor deposition.

semiconductor film layer is maintained chemically active.

Next, an adsorption layer containing boron, element or boron compound is formed on the active surface of the silicon semiconductor film layer. For example, while the substrate temperature is maintained at 825°C, diborane gas ( $B_2H_6$ ) containing boron is applied to the surface of the silicon substrate 1. The diborane gas diluted with nitrogen carrier gas at 5% is introduced into the chamber for a predetermined time interval so as to fill the chamber at  $1.3 \times 10^2 Pa$  of the internal pressure to thereby form the boron-containing adsorption layer.

Lastly, the diffusion treatment is carried out such that the diborane gas is stopped after formation of the impurity adsorption layer, and the substrate is annealed in vacuum to effect solid-phase diffusion of the boron from a diffusion source in the form of the adsorption layer. Concurrently, the diffused impurity atoms are activated in the silicon film layer.

Fig. 4 shows an impurity diffusion density profile in the thus obtained base region. This profile is obtained by a secondary ion mass-spectrometer. A surface of the sample substrate is coated by an amorphous silicon layer in order to improve analysis accuracy on the sample surface. Therefore, in the Fig. 4 profile, the original surface level of the semiconductor film layer diffused with the impurity is indicated at a boundary between the amorphous silicon layer and the semiconductor film layer. The semiconductor film layer, i.e., epitaxial layer is uniformly doped with the impurity boron as shown in the profile. The impurity density profile steeply falls at a PN junction region between the lower collector region and the upper base region. As described above, according to the first aspect of the invention, the impurity diffusion is accurately controllably effected to the significantly thin epitaxial layer while regulating the impurity distribution profile in the depth direction.

Fig. 5 is a graph showing the relation between the boron peak density in the base region, and the application pressure ( $P_1, P_2, P_3$ ) and application time interval of diborane gas. As shown in the graph, the higher the application pressure of diborane gas, the more the boron peak density. The longer the application time interval, also the more the boron peak density. In this manner, by suitably setting the application condition of diborane gas, the boron impurity concentration can be controlled in the base region.

In the above described embodiment, the P type impurity of boron is diffused into the silicon semiconductor film layer so as to form a P type base region of NPN bipolar transistor. The doping of P type impurity can be effected with using various source gases of III-group element com-

ound such as trimethyl gallium (TMG) and boron trichloride ( $BCl_3$ ) besides the above described diborane gas. On the other hand, in order to dope an N type impurity into a silicon semiconductor film layer to form an N type base region of PNP bipolar transistor, there may be utilized various impurity gases such as arsine ( $AsH_3$ ), phosphorus trichloride ( $PCl_3$ ), antimony pentachloride ( $SbCl_5$ ) and phosphine ( $PH_3$ ). The substrate temperature is set to 825°C in the embodiment. According to the inventors' study, the substrate temperature should be set in the range from 800°C to 1200°C optimally in conjunction with the background pressure and ambient gas species for the surface cleaning treatment. The substrate temperature should be preferably set in the range from 400°C to 950°C for the formation of impurity adsorption film. Further, the substrate temperature should be preferably set in the range from 800°C to 1100°C for the epitaxial growth of the semiconductor film layer.

As described above, according to the first aspect of the invention, an impurity adsorption layer is directly formed on a semiconductor film layer deposited on a collector region, and solid-phase diffusion is effected from a diffusion source in the form of the adsorption layer so as to intensively and limitatively dope the impurity into the semiconductor film layer to thereby form therein a base region. Consequently, the thickness of the base region can be considerably reduced as compared to the prior art, thereby advantageously increasing operating speed of bipolar transistor.

The next description is given for the second embodiment of producing a PNP bipolar transistor in conjunction with Figs. 6A - 6F. In the first step of Fig. 6A, a collector region 102 is formed on a semiconductor substrate 101 composed of silicon. The collector region 102 has a double layer structure composed of a first diffusion layer 103 doped with high density of P type impurity and a second diffusion layer 104 doped with moderate density of the same P type impurity. The high density first diffusion layer 103 is provided to reduce collector-series resistance of a bipolar transistor, and the upper second diffusion layer 104 of P type is provided to form a PN junction. A field oxide film 105 is formed on the collector region 102. This field oxide film 105 is provided to isolate from each other a plurality of bipolar transistors integrated on the semiconductor substrate 101. The field oxide film 105 surrounds each device region. The field oxide film 105 is formed by, for example, selective thermal oxidation.

In the Fig. 6B step, the collector region 102 is covered by a first semiconductor film layer 106 composed of silicon. This first semiconductor film layer 106 is deposited by, for example, epitaxial

polar transistor.

5

10

15

20

25

30

35

40

45

50

55

FIG. 2

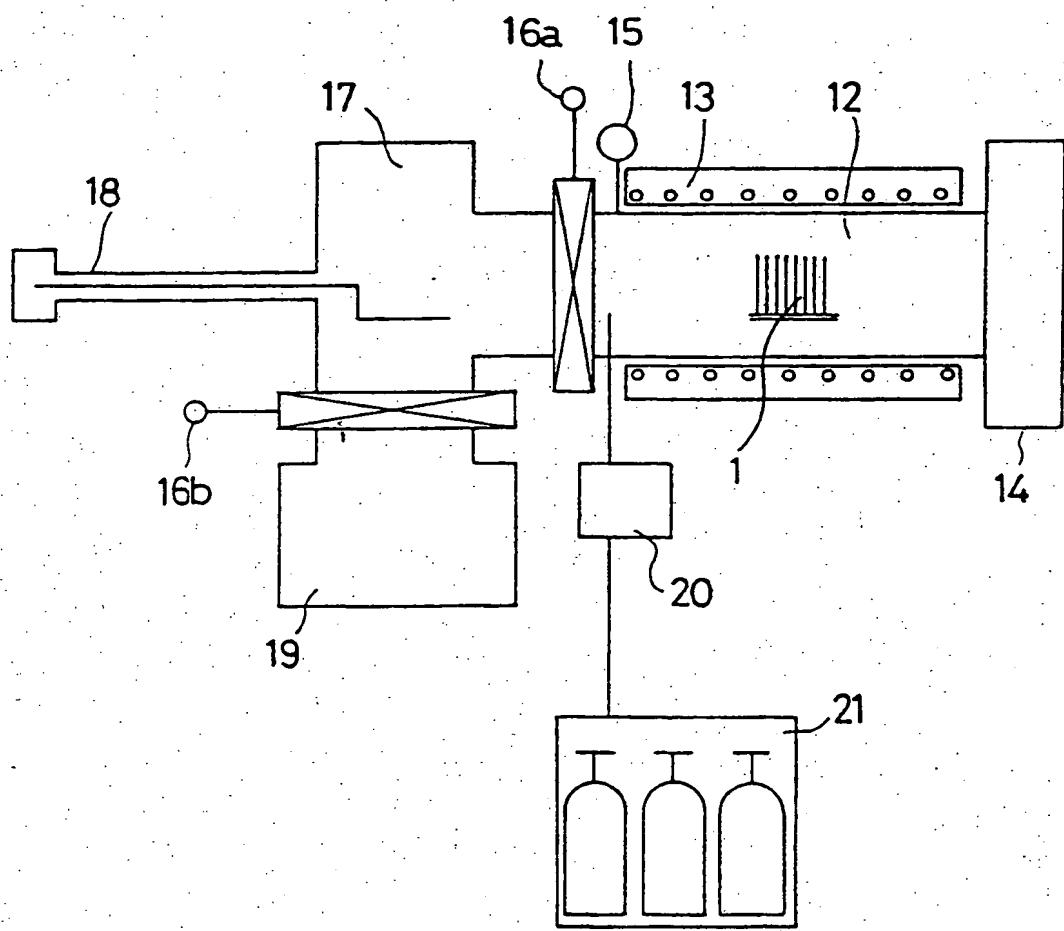


FIG. 5

